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09/723,795	11/27/2000	Kenneth D. Easton	PA990097	6015

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Qualcomm Incorporated
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EXAMINER	
LIU, SHUWANG	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/723,795	EASTON ET AL.	
	Examiner	Art Unit	
	Shuwang Liu	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39,43,44,47-54 and 57- 59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 35* is/are allowed.

6)☒ Claim(s) *1-14,16-34,36-39,43,44,47-54 and 57-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. The request filed on June 18, 2001, for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/723,795 is acceptable and a RCE has been established. An action on the RCE follows.

Response to Arguments

2. Applicant's arguments filed on 06/18/04 have been fully considered but they are not persuasive. The Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

Applicant's argument – "Kawable process multiple copies of the same signal in parallel is different than processing them in a serial fashion as claimed by Applicant."

Examiner's response – As agreed by the Applicant, Kawable does teach the concept of time sharing a rake receive between multiple signals, the data retrieved from memory includes all multipaths of a signal transmission instead of "the same signal". The data retrieved from memory are fed not simultaneously into a parallel arrangement of finger processor because the processing on a plurality of channels is accomplished by time division multiplexing by a signal processing apparatus provided with the memory (column 2,lines 36-46). In response to applicant's argument that the references fail to show certain features

of applicant's invention, it is noted that the features upon which applicant relies (i.e., processing "segments" in a serial fashion) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-14, 16-34, 36-39, 43, 44, 47-54, 57 and 58 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification does not describe that "the data processor is further operative to process two or more of the retrieved segments at different times with the same corresponding segment of a dispreading sequence." The specification only describes "a segment of PN samples can be retrieved from buffer 224 and

used to despread a corresponding segment of data samples" (page lines 17-19 on page 19).

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-14, 16-34,, 36-39, 43, 44, 47-54, 57 and 58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims recite the limitation " the same corresponding segment of a dispreading sequence " in line 8 of claim 1, line 10 of claim 47 and line 9 of claim 48. There is insufficient antecedent basis for this limitation in the claim since the limitation is not introduced before.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 1-3, 7-10, 12, 13, 25, 38, 47-49 and 58 are rejected under 35 U.S.C. 102(a) as being anticipated by Lee (EP 1017183A2).

As shown in figures 1-6, Lee discloses a receiver unit and a method for processing a received signal in a wireless communications system, comprising:

(1) regarding claims 1, 47 and 48:

a first buffer (322) operative to receive and store digitized samples comprising multiple instances of a received signal; and

a data processor (310 and 320) coupled to the first buffer and operative to retrieve different segments of digitized samples from the first buffer, each of the retrieved segments comprising one of the signal instances, wherein the data processor is further operative to process two or more of the retrieved segments at different times with a same corresponding segment of a dispreading sequence programmed into the data processor to provide correlated samples (column 6, line 19-column 8, line 15 and figure 5).

(2) regarding claim 2:

further comprising: a controller (316) coupled to the data processor and operative to dispatch tasks for the data processor and to process signaling data from the data processor (column 5, lines 32-43).

(3) regarding claim 3:

wherein the controller is operative to direct processing of the segments of digitized samples (column 5, lines 41- column6, line 30).

(4) regarding claim 7:

further comprising: a receiver (figure 1) operative to receive and process a transmitted signal to provide the digitized samples (106 and figure 4).

(5) regarding claims 8 and 49:

wherein the data processor includes a correlator (110 or figure 6) operative to despread the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples.

(6) regarding claim 9:

wherein the data processor further includes a symbol demodulation and combiner (110 and 116) coupled to the correlator and operative to receive and process the correlated samples to provide processed symbols (figure 4 and figure 6).

(7) regarding claim 10:

wherein the data processor further includes an accumulator (504 in figure 6, 904 in figure 7, 604 in figure 8, or 705 in figure 9) coupled to the correlator and operative to receive and process the correlated samples to provide accumulated results.

(8) regarding claim 12:

wherein the correlator includes a set of K multipliers (604, 606, 604, 602 and 600) operative to concurrently despread sets of up to K complex digitized samples (figure 6).

(9) regarding claim 13:

wherein the correlator further includes a set of K summers (608) coupled to the set of K multipliers, each summer operative to receive and sum pairs of samples from two multipliers (figure 6).

(10) regarding claim 25:

wherein the accumulator is operative to accumulate the correlated samples over a programmable time interval to provide pilot signal estimates (column 12, lines 9-35).

(11) regarding claim 38:

wherein the first buffer is operative to store two or more packets of digitized samples (figure 4).

(12) regarding claim 58:

wherein the data processor is further configured to coherently combine (116 or 610) the correlated samples from the two or more of the segments to generate processed symbols.

9. Claims 1-3, 7-13, 23-26, 32, 36-38, 43, 44, 47-49, 54 and 58 are rejected under 35 U.S.C. 102(a) as being anticipated by Kawabe et al. (EP 0998052A2) (whereby, "with the same corresponding segment of a dispreading sequence" is interpreted to be - -with a corresponding segment of a dispreading sequence- -).

As shown in figures 1-10, Kawable et al. discloses a receiver unit and a method for processing a received signal in a wireless communications system, comprising:

(1) regarding claims 1, 47 and 48:

a first buffer (203-1-3 in figure 1 or 402 in figure 5) operative to receive and store digitized samples comprising multiple instances of a received signal (column 2, lines 36-46 and column 4, line 54-column 5, line 55); and

a data processor (202 in figure 2 or 403 in figure 5) coupled to the first buffer and operative to retrieve different segments of digitized samples from the first buffer (column 2, lines 36-46 and column 4, line 54-column 5, line 55), each of the retrieved segments comprising one of signal instances, wherein the data processor is further operative to process two or more of the retrieved segments at different times with a corresponding segment of a dispreading sequence programmed into the data processor to provide correlated samples (column 11, line 57-column 12, line 7).

(2) regarding claim 2:

further comprising: a controller (401) coupled to the data processor and operative to dispatch tasks for the data processor and to process signaling data from the data processor (column 9, lines 28-36).

(3) regarding claim 3:

wherein the controller is operative to direct processing of the segments of digitized samples (column 9, lines 28-36).

(4) regarding claim 7:

further comprising: a receiver (201) operative to receive and process a transmitted signal to provide the digitized samples (column 4, lines 46-49 and column 5, lines 44-47).

(5) regarding claims 8 and 49:

wherein the data processor includes a correlator (208-1-n or 503 in figure 6) operative to despread the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples (column 8, lines 5-9).

(6) regarding claim 9:

wherein the data processor further includes a symbol demodulation and combiner (214) coupled to the correlator and operative to receive and process the correlated samples to provide processed symbols (column 6, lines 9-21).

(7) regarding claim 10:

wherein the data processor further includes an accumulator (504 in figure 6, 904 in figure 7, 604 in figure 8, or 705 in figure 9) coupled to the correlator and operative to receive and process the correlated samples to provide accumulated results.

(8) regarding claim 11:

wherein the data processor further includes a second buffer (404) coupled to the symbol demodulation and combiner and operative to store the processed symbols (column 9, lines 40-53).

(9) regarding claim 12:

wherein the correlator includes a set of K multipliers (208-1, 208-2,... or 903-1, 903-2, .. in figure 7 or 704 in figure 9) operative to concurrently despread sets of up to K complex digitized samples (column 12, line 51-column 13, line 23).

(10) regarding claim 13:

wherein the correlator further includes a set of K summers (705) coupled to the set of K multipliers, each summer operative to receive and sum pairs of samples from two multipliers (column 12, line 51-column 13, line 23).

(11) regarding claim 23:

wherein the second buffer is operative to provide the processed symbols to a subsequent signal processing element (215 or 407)in an output order that is different from an input order to provide de-interleaving of the processed symbols (column 6, lines 22-25 and column 14, lines 3-15).

(12) regarding claim 24:

It is inherent that the second buffer includes at least two sections, one section operative to store processed symbols for a current packet (current slot) being processed and another section operative to store processed symbols for a prior processed packet (prior slot) to be provided to the subsequent signal processing element (column 9, lines 3-13).

(13) regarding claim 25:

wherein the accumulator is operative to accumulate the correlated samples over a programmable time interval to provide pilot signal estimates (column 12, lines 9-35).

(14) regarding claim 26:

wherein the accumulator includes a plurality of accumulate elements (504 and 505 in figure 7, or 904-1, 904-1, ...905-1, 905-2, ... in figure 7), each accumulate element operative to provide pilot signal estimate for a particular time offset (column 12, lines 9-35).

(15) regarding claim 32:

wherein the sample rate is asynchronous with the processing clock (column 9, lines 27-37).

(16) regarding claim 36:

further comprising: a data interface (201)coupled to the first buffer, the data interface operative to receive the digitized samples, discard unnecessary samples, and assemble the samples into words suitable for efficient storage to the first buffer.

(17) regarding claim 37:

wherein a word of 32 bits (for w-cdma) or more is written to the first buffer or read from the first buffer for each buffer access (column 4, line 54-column 5, line 355).

(18) regarding claim 38:

wherein the first buffer is operative to store two or more packets of digitized samples (column 4, line 54-column 5, line 55).

(19) regarding claim 43:

wherein the frequency of the processing clock is at least ten times higher than the sample rate (column 5, lines 44-55).

(20) regarding claim 44:

wherein the wireless communications system is a high data (HRD) CDMA system (WCDMA) (column 4, line 54-58 and column 5, lines 44-55).

(21) regarding claim 54:

the processing of the signal instances includes dispreading the retrieved segment of the digitized samples with corresponding segment of PN dispreading sequence to provide correlated samples (column 11, lines 35-column 12, 36).

(22) regarding claim 58:

wherein the data processor is further configured to coherently combine (214 or 504 or 904) the correlated samples from the two or more of the segments to generate processed symbols.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 4-6, 14, 16-22, 27, 28, 50-52, 57 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawabe et al. in view of Subramanian et al. (US 6,459,883).

(1) regarding claims 4-6, 27, 28, 57 and 59:

Kawabe et al. discloses all of the subject matter as described above except for specifically teaching the controller operating to instantiate a timing state machine for each signal instance being processed, wherein state machine

includes a time tracking loop operative to track movement of the signal instance being processed as recited in the claims.

Subramanian et al., in the same field of endeavor, teaches a controller (116, 118, 120 and 122 in figure 1) having a timing state machine includes a time tracking loop operative to track movement of the signal instance being processed (abstract, column 3, lines 1-55, figures 8-12).

It would be desirable to provide flexible and programmable generic rake receiver architecture suitable for different spread spectrum system at a minimal development cost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use controller as taught by Subramanian et al. to implement the controller of Kawabe et al. in order to provide an integration of generic, inexpensive components in a fully configurable manner.

(2) regarding claims 16-20 and 50:

Kawabe et al. discloses all of the subject matter as described above except for specifically teaching the demodulator including a decover element operative to receive and decover the correlated samples with one or more Walsh codes to provide decovered symbols.

Subramanian et al., in the same field of endeavor, teaches a dechannelizer (110-114 in figure 1, 708, 710 in figure 7 and 928, 930 and 932 in figure 9) to decover the correlated symbols with Walsh codes (711), wherein the decover is implemented with a FHT (column 8, lines 40-45) operating for inphase and quadrature samples (see figure 7). Furthermore, it is inherent for WCDMA

that the FHT element is operative to perform decovering with one or more Walsh symbols of a length of 1, 2, 4, 8, 16, 32, 64, or 128.

Although Kawable did not teach orthogonal Walsh channelization, Subrammanian et al. teach using dechannelization means by orthogonal Walsh code for separate channels (110-114 in figure 1 and figure 7). It is also well known that the orthogonal sequences currently used in CDMA system are Walsh codes of length 64. Walsh codes are used in forward CDMA link to separate users. In any given sector, each forward code channel is assigned a distinct Walsh code. The receiver despreads the chips by using the same Walsh code used at the transmitter so that the symbols or digits are recovered without any error. When the wrong Walsh sequence is used for dispreading, the resulting correlation yields an average of zero. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use orthogonal Walsh code as taught by Subrammanian et al. in the demodulator of Kawable to perform the channelization in the CDMA receiver. In so doing, the receiver facilitates separating different users from the composite spread signal so that the channel security is improved and the data can be recovered without errors.

(3) regarding claims 21, 22, 51 and 52:

Kawabe et al. discloses all of the subject matter as described above except for specifically teaching the demodulator including a pilot demodulator coupled to the decover element and operative to demodulate the decovered symbols with pilot symbols to provide demodulated symbols.

Subramanian et al., in the same field of endeavor, teaches a pilot demodulator (figure 10) coupled to the decover element and operative to demodulate the decovered symbols with pilot symbols to provide demodulated symbols (column 8, line 64-column 8, line 18). Furthermore, Subramanian et al. teaches the demodulator including a symbol accumulator (1012) coupled to the pilot demodulation and operative to accumulate the demodulated symbols from multiple signal instances to provide the processed symbols (column 9, lines 19-27).

It is also well known that the pilot signals are used in transmission protocols to help the receiver estimate an unknown channel. If the transmitter sends out a known pilot signal with a known PN sequence, then the receiver can determine the phase correction using an internally generated PN sequences that is identical to that of the transmitter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use pilot signal as taught by Subrammanian et al. in the demodulator of Kawable to determine phase estimation and correction in the CDMA receiver. In so doing, the receiver facilitates separating different users from the composite spread signal so that the channel security is improved and the data can be recovered without errors.

(4) regarding claim 14:

Kawabe et al. discloses all of the subject matter as described above except for specifically teaching the correlator including an interpolator operative

to receive and interpolate despread samples from the PN despreading to generate interpolated samples that are provided as the correlated samples.

Subramanian et al., in the same field of endeavor, teaches the correlator (910 and 902 in figure 9) includes an interpolator (902).

It should be noted that the arrangement of the blocks in Subramanians' correlator differs from claim 12 of the present invention. Subramanian et al. reversed the order of the despreader (910) and interpolator (902) recited. The order of despreader and interpolator does not affect the result of the output of the correlator because the two arrangements are art-recognized functional equivalents.

The interpolator is conventionally known in the art and discussed in John G. Proakis, Digital Communications, 2nd edition, McGraw-Hill, 1989. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the interpolator as taught by Subrammanian et al. in the correlator of Kawable to adjust the timing of the correlated signal. In so doing, the receiver facilitates timing adjustment from the spread signal so that the data can be recovered without errors.

Allowable Subject Matter

12. Claims 15 and 35 are allowed.

13. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach and suggest the receiver comprises the interpolator including one or more pairs of scaling elements, each scaling element operative to receive and scale respective despread samples with a particular gain to generate scaled samples, and one or more summer, each summer coupled to a respective pair of scaling elements and operative to receive and sum the scaled samples from the pair of scaling elements to generate the interpolated samples as received in claim 15. Furthermore, the prior art fails to teach and suggest the receiver comprises the micro-controller includes a set of latches operative to latch a dispatched task and one or more parameter values to be applied for the dispatched task, at least one counter, each counter coupled to a respective latch and operative to provide an indicator signal based on a value stored in the latch, and a sequencing controller operative to receive at least one indicator signal and the dispatched task and to generate the set of control signals as recited in claim 35.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shuwang Liu whose telephone number is (571) 272-3036.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin, can be reached at (571) 272-3056.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Shuwang Liu
Primary Examiner
Art Unit 2634

August 30, 2004